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09/538,012	03/29/2000	Carole Dulong	42390.P6156	6257

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EXAMINER	
COLLINS, SCOTT M	

ART UNIT	PAPER NUMBER
2143	14

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No. 09/538,012	Applicant(s) DULONG, CAROLE	
	Examiner Scott M. Collins	Art Unit 2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: One month Extension of Time and Amendment D on 01/12/2004.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-7 and 14-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, claims 1 and 14 include the limitation "computing addresses comprises executing a first plurality of instructions to transfer a plurality of said indices from a first storage location where the indices are stored substantially contiguously, to an equal plurality of separate storage locations, wherein each index is assigned its own separate storage location". However, the specification does not disclose this limitation nor does the specification explain how addresses are computed simply by storing data.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-7 and 14-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. Specifically, claims 1 and 14 claim that addresses are somehow computed by storing data. Normally, computing any type of data involves a computation and not simply a data transfer.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-4, 8-11, 14-17, and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Austin et al., U.S. Patent Number 3,163,850 (herein referred to as Austin).

9. Referring to claim 1, Austin has taught a method for performing a gather operation on a computer processor comprising:

a. computing addresses for a plurality of data elements of a matrix stored in a memory wherein each data element is identified by one of a plurality of indices and a base address (Austin column 1, line 25 – column 2, line 50; column 5, lines 49-70; and figure 1, address adder 103 with inputs: increment value 101 and start address 52);

b. retrieving each of said data elements from memory based on the computed addresses (Austin column 5, lines 49-73); and

c. executing a second plurality of instructions, each instruction depositing one or more of said data elements contiguously with other data elements in a second storage location (Austin column 5, lines 49-73).

10. Further, it can be seen from Austin column 1, lines 10-24, column 2, lines 56-57 and column 6, lines 40-42 that Austin expressly discloses the scattering RSV instruction while not fully disclosing the details of the gathering RGV instruction since it is simply the inverse of the fully disclosed scattering RSV instruction.

11. It should be noted that remaining limitations have been addressed in the 35 U.S.C. 112 rejection above.

12. Referring to claims 2 and 15, Austin has taught the method and the computer system wherein said storage locations are registers (Austin column 1, lines 25-35, column 5, lines 49-73 and figure 1, elements 19, 52, 75. It should also be noted that the basic data storage unit is a register and would inherently be used to store these data elements).

13. Referring to claims 3 and 16, Austin has taught the method and the computer system wherein computing addresses further comprises:

a. extracting indices for each of said data elements into separate storage locations (Austin column 5, lines 62-70 and figure 1, increment value 101 acting as a calculated index); and

b. adding each of said indices to a base address (Austin column 5, lines 62-70 and figure 1, address adder 103 and start address 52 which acts as a base address.).

14. Referring to claims 4 and 17, Austin has taught the method and the computer system further comprising loading each of said data elements from memory into separate storage locations prior to executing said second plurality of instructions (Austin column 2, lines 51-57, column 5, lines 49-70. Further, it can be seen from Austin column 2, lines 56-57 and column 6, lines 40-42 that Austin expressly discloses the scattering RSV instruction while not fully

disclosing the details of the gathering RGV instruction since it is simply the inverse of the fully disclosed scattering RSV instruction.).

15. Referring to claim 8, Austin has taught a method for performing a scatter operation on a computer processor comprising:

a. calculating addresses in memory to which a plurality of data elements are to be scattered to form a matrix in memory wherein each address in memory is identified by one of a plurality of indices and a base address (Austin column 1, line 25 – column 2, line 50; column 5, lines 49-70; and figure 1, address adder 103 with inputs: increment value 101 and start address 52);

b. executing a plurality of extract instructions, each of said extract instructions extracting one or more of said data elements from a separate storage location in which said data elements are stored contiguously to an equal plurality of separate storage locations (Austin column 5, lines 49-73); and

c. transferring said data elements from said separate storage locations to said calculated addresses in memory (Austin column 5, lines 49-73).

16. Referring to claim 9, Austin has taught the method wherein each of said storage locations are registers (Austin column 1, lines 25-35, column 5, lines 49-73 and figure 1, elements 19, 52, 75. It should also be noted that the basic data storage unit is a register and would inherently be used to store these data elements).

17. Referring to claim 10, Austin has taught the method wherein calculating addresses comprises:

a. extracting indices for each of said data elements into separate storage locations (Austin column 5, lines 62-70 and figure 1, increment value 101 acting as a calculated index); and

b. adding each of said indices to a base address (Austin column 5, lines 62-70 and figure 1, address adder 103 and start address 52 which acts as a base address.).

18. Referring to claim 11, Austin has taught the method wherein storing each of said data elements is accomplished via a plurality of STORE instructions executed by said computer processor (Austin column 5, lines 49-55 where Austin's RSV instruction corresponds to applicant's EXTRACT instruction.).

19. Referring to claim 14, Austin has taught a computer system comprising:

a. a memory (Austin figure 1, memory 16);

b. a processor communicatively coupled to the memory (Austin figure 1, all elements beside memory 16 comprise the processor); and

c. a storage device communicatively coupled to the processor and having stored therein a sequence of instructions (Austin figure 1, memory 16 and column 1, lines 10-35) which, when executed by the processor, causes the processor to at least,

1. compute addresses for a plurality of data elements of a matrix stored in memory wherein each data element is identified by one of a plurality of indices and a base address (Austin column 1, line 25 – column 2, line 50; column 5, lines 49-70; and figure 1, address adder 103 with inputs: increment value 101 and start address 52);

2. retrieve each of said data elements from memory based on the computed addresses (Austin column 5, lines 49-73); and

3. execute a second plurality of instructions, each instruction to deposit one or more of said data elements contiguously with other data elements in a storage location (Austin column 5, lines 49-73).

20. Referring to claim 21, Austin has taught the method wherein computing addresses comprises executing a series of instructions, each instruction to extract an address index for one of said plurality of data elements (Austin column 5, lines 71-73 where execution of the instruction is repeated until address computation is complete.).

21. Referring to claim 22, Austin has taught the method wherein said address indices are extracted from a series of contiguous memory locations (Austin column 5, lines 49-70 where Austin's RSV scatter instruction takes a contiguous set of memory and scatters it to a discontiguous set of memory.).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 5, 7, 12, 13, 18, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Austin et al., U.S. Patent Number 3,163,850 (herein referred to as Austin).

24. Referring to claims 5, 12, and 18, Austin has not disclosed the method nor the computer system wherein said computer processor executes two or more of said first and/or second

plurality of instructions in a single clock cycle. However, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to implement this scatter method in a modern superscalar computer system having an IPC (instructions per clock) of less than 1. One of ordinary skill in the art would have been motivated to do this in order to have a faster and more efficient processing system.

25. Examiner takes Official Notice (see MPEP § 2144.03) that "superscalar computing" in a computing environment was well known in the art at the time the invention was made. The Applicant is entitled to traverse any/all official notice taken in this action according to MPEP § 2144.03. However, MPEP § 2144.03 further states "See also In re Boon, 439 F.2d 724, 169 USPQ 231 (CCPA 1971) (a challenge to the taking of judicial notice must contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial notice)." Specifically, In re Boon, 169 USPQ 231, 234 states "as we held in Ahlert, an applicant must be given the opportunity to challenge either the correctness of the fact asserted or the notoriety or repute of the reference cited in support of the assertion. We did not mean to imply by this statement that a bald challenge, with nothing more, would be all that was needed". Further note that 37 CFR § 1.671(c)(3) states "Judicial notice means official notice". Thus, a traversal by the Applicant that is merely "a bald challenge, with nothing more" will be given very little weight.

26. Referring to claims 7, 13, and 20, Austin has not disclosed the method nor the computer system wherein said registers are 64-bits wide and said data elements are 16-bits in length. However, at the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to store data elements of 16-bits length in 64-bit

wide registers, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

27. Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Austin et al., U.S. Patent Number 3,163,850 (herein referred to as Austin) in view of McDonnell et al., U.S. Patent Number 2,968,027 (herein referred to as McDonnell).

28. Referring to claims 6 and 19, McDonnell has taught the method and the computer system further comprising storing each of said data elements on a mass storage device (McDonnell column 7, lines 23-28 and figure 1a, tape units 1-6). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to include a mass storage device as McDonnell has disclosed in the gather-scatter system Austin has disclosed. A person of ordinary skill in the art would have found it obvious to use a more modern mass storage device – such as a hard disk, etc. – as opposed to McDonnell's tape units. One of ordinary skill in the art would have been motivated to incorporate this portion of McDonnell's system into Austin's system because Austin repeatedly points a reader of his patent to McDonnell's system as the basis of his system (Austin column 1, lines 19-24, column 2, lines 33-38 and 45-46, column 3, lines 56-57).

Response to Arguments

29. Applicant's arguments filed 01/12/2004 have been fully considered but they are not persuasive. Applicant's main argument is that the invention "does not require dedicated hardware." However, this has not been claimed in any way. Applicant claims that a plurality of instructions is used, but these instructions inherently utilize hardware – albeit not necessarily dedicated hardware. Applicant also emphasizes the use of a plurality of instructions as opposed to a singular instruction, but applicant is referred to column 5, lines 71-73 of Austin where an execution is repeated until a task is completed.

Conclusion

30. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott M. Collins whose telephone number is 703.305.7865. The examiner can normally be reached on Mon.-Fri. 8:00 am - 5:30 pm with alt. Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A Wiley can be reached on 703.308.5221. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.305.3900.

smc
March 8, 2004

DAVID WILEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100